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Date: 12/1/03

John M. Ling

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Applicant(s): Gary Dan Dotson *et al.*

Serial No: 09/672,637

Filing Date: September 28, 2000

Examiner: Thu Thao Havan

Art Unit: 2672

Title: MULTIPLE COLOR DEPTH DIGITAL DISPLAY INTERFACE

MS Appeal Brief - Patents
Commissioner for Patents
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

Applicants submit this brief in triplicate in connection with an appeal of the above-identified application. The Commissioner is authorized to charge $330.00 for the fee associated with this brief to Deposit Account No. 50-1063, Order No. ALBRP203US.

I. Real Party in Interest (37 C.F.R. § 1.192(c)(1))

The real party in interest in the present appeal is ROCKWELL TECHNOLOGIES, LLC, the assignee of the present application.

II. Related Appeals and Interferences (37 C.F.R. § 1.192(c)(2))

Appellants, appellants' legal representatives, and/or the assignee of the present application are unaware of any appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims (37 C.F.R. § 1.192(c)(3))

Claims 1-33 are pending in the application. The rejections of claims 1-33 are appealed.

IV. Status of Amendments (37 C.F.R. § 1.192(c)(4))

No claims amendments have been made subsequent to the final rejection of June 2, 2003.

V. Summary of Invention (37 C.F.R. § 1.192(c)(5))

The present invention relates generally to the field of video displays and more particularly to an improved raster engine with a multiple color depth digital display interface. Independent claim 1 recites "A raster engine for interfacing a frame buffer in a computer system to one of a plurality of disparate displays, comprising: at least one ***control register programmable via the computer system to select a display mode***; a *dual port RAM device operative to obtain pixel data from the frame buffer*; and a logic device having a *parallel output*, the logic device being ***adapted to select appropriate pixel data*** from the dual port RAM device ***according to the selected display mode, to remap the selected pixel data according to the selected display mode***, and to provide remapped selected pixel data at the parallel output according to a universal routing scheme applicable ***to the plurality of disparate displays***." Independent claims 20, 26, and 30 recite similar aspects. "Disparate" is defined as "markedly distinct in quality or character." As used in the subject claim, disparate can mean for example, an HDTV device and an LCD device, which are markedly distinct from each other in terms of their graphical resolution capabilities. The raster engine of the subject claims "*is easily programmed to interface* a computer system running a variety of application programs *with a plurality of disparate display types*. The invention can thus be employed in high end as well as highly cost sensitive computer system applications in association with displays *ranging from high definition television (HDTV) to low resolution monochrome EL and/or LCD display panels*." (Page 4, lines 26-31.) The raster engine of the

subject claims is capable of ***selecting a display mode***. (*See, e.g.*, Claims 1, 21, 26, and 30.) "In addition, the raster engine can further comprise an integrated digital to analog converter (DAC) to support analog LCD displays and CRTs." (Page 9, lines 13-14.) Furthermore, "[p]rogrammable compare and register logic 4 *allows a user or a host system application program to* ***select appropriate display modes*** for interfacing a frame buffer with ***one or a plurality of disparate display devices***." (Page 16, lines 23-25.) Thus, the subject claims recite a system capable of selecting display modes for simultaneously displaying data on a variety of different types of (*e.g.* "disparate") displays.

VI. Statement of the Issues (37 C.F.R. § 1.192(c)(6))

Whether claims 1-33 are patentable under 35 U.S.C. §103(a) over U.S. Patent No. 6,157,393 to Potter *et al.* in view of U.S. Patent No. 5,321,809 to Aranda.

VII. Grouping of Claims (37 C.F.R. § 1.192(c)(7))

For the purposes of this appeal only, the claims are grouped as follows:

Claims 1-33 stand or fall together.

VIII. Argument (37 C.F.R. § 1.192(c)(8))

Rejection of claims 1-33 Under 35 U.S.C. §103(a)

A. Potter et al. fails to describe, either expressly or inherently, each and every element of the claimed invention as set forth in the subject claims. Specifically, Potter et al. fails to teach or suggest a control register that indicates and/or selects a display mode, parallel outputs, or formatting data in a manner suitable for rendering on a plurality of disparate display device types.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) ***must***

> ***teach or suggest all the claim limitations***. *See* MPEP §706.02(j). The ***teaching or suggestion to make the claimed combination*** and the reasonable expectation of success ***must both be found in the prior art and not based on applicant's disclosure***. *See In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added).

The Examiner contends in the Advisory Action that the "plurality of disparate displays" has not been given patentable weight because the recitation occurs in the preamble, which is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness. Applicant's representative respectfully points out that "*a* plurality of disparate displays" that is mentioned in the preamble of claim 1 is antecedent basis for "*the* plurality of disparate displays" referred to in the last line of claim 1, which receives remapped pixel data from a logic device having a parallel output. Thus, the body of claim 1 depends on the preamble for completeness (*e.g.*, for antecedent basis), and claim 1 recites outputting remapped selected pixel data to a plurality (*e.g.*, more than one) of disparate display devices.

As stated in the Reply to Advisory Action Dated September 4, 2003, Potter *et al.* merely describes a system that directs graphical data to *a* display device 170. Contrary to the Examiner's assertion, the "bus controller 125...provided for controlling a bus 130" (Column 5, lines66-67) does *not* teach or suggest the limitation of a control register able to ***select*** or ***indicate a display mode***. Furthermore, according to Potter *et al.*, "The display device 170 preferably is a conventional horizontal scan cathode ray tube ("CRT") monitor having a plurality of pixels." (Column 6, lines 30-32.) Potter *et al.* discusses displaying data *across* two or more display devices. (*See, e.g.*, Column 14, lines 28-34.) However, such display of data is merely a *single set of data* that is *formatted in a single predetermined manner* and divided for display on more than one of the same type of display device, such as two CRTs, but not a CRT and another different type of display device. The referenced discussion of plural display devices does not teach or suggest a system capable of *selecting a display mode* and *formatting data* in a manner suitable for concurrent rendering on a ***plurality of disparate display device types***. Thus, Potter *et al.* fails to teach or suggest all of the claim limitations of the subject application as recited in independent claims 1, 21, 26, and 30.

The Examiner goes on to state that "*a logic device having a parallel output*" is disclosed at (col. 7, lines 50-67) in Potter. To the contrary, Potter merely teaches "a plurality of parallel gradient producing units 210" (col. 7, lines 53-54) and "parallel rasterizers 214" (col. 7, line 61), but does *not* teach "*a logic device having a parallel output*." Thus, Potter does *not* teach this aspect of the present invention.

The Examiner further states that "the logic device being adapted to select appropriate pixel data from the dual port RAM device according to the selected display mode" is found at (col. 8 line to col. 10, line 23; col. 14, lines 28-64; fig. 3a). The cited sections of Potter *et al.* merely disclose RAMDACS, which convert digitally encoded images into analog signals that can be displayed by a monitor. Independent claim 1 recites, "the logic device being adapted to select appropriate pixel data ***from the dual port RAM device according to the selected display mode***." Potter is *outputting to* the RAMDACs to convert digital signals to analog for a display. The present invention's logic device *receives* data *from* a dual port RAM device *according to a selected display mode*. Thus, Potter does *not* disclose this aspect of the present invention and actually *teaches away from* the present invention.

Aranda fails to make up for the aforementioned deficiencies of Potter *et al.* Aranda's discussion of a display interface states: "The display interface operates to generate the analog signals RGB on line 21 necessary to display the image on ***a*** display device (or CRT) 16 (along with the appropriate control signals). Although a CRT or monitor device is shown in the preferred embodiment, the techniques employed herein work equally well for ***any two-dimensional display device*** such as ***a*** plotter, printer, or other monitor type." (Column 5, lines 16-23, emphasis added.) Thus, Aranda merely discloses displaying data in a *single format* on a *single type* of display device at any single given time, as shown by the above-emphasized language. Aranda does not teach or suggest *selecting display modes* for *simultaneously displaying data on a plurality of* ***disparate*** *devices*. Nor does Aranda teach or suggest a parallel output or a control register that selects and/or indicates a display mode.

B. Aranda teaches away from a single, two-port RAM device.

> To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the examiner to show a motivation to combine the references that create the case of obviousness. In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet*, 149 F.3d 1350, 1357.
>
> A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)

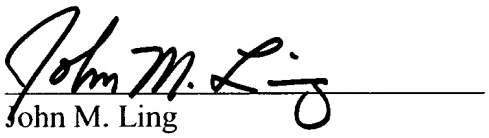
Moreover, Aranda *teaches away* from several aspects of the present invention. Specifically, Aranda discusses the *impracticability* of separating the frame buffer into two separate devices. The Examiner has stated that "it would have been obvious to combine the teaching of Aranda to the system of Potter because doing so would have *enabled* dividing the entire frame buffer into two separate devices so that the characteristics of adjacent pixels can be alternately stored in different ones of the two devices as noted in Aranda (col. 1, line 15 to col. 2, line 33)." Applicants respectfully point out that Aranda actually states, "The most straightforward approach to improving performance is to *divide the entire frame buffer into two separate devices* so that the characteristics of adjacent pixels can be alternately stored in different ones of the two devices." (col. 2, lines 22-26) (emphasis added). But, more importantly, Aranda then states, "The *difficulty with this approach*, however, is that twice the number of pins are required of the raster engine to access the dual devices. This requirement proves in practice to be a *significant complication*." (col. 2, lines 28-32) (emphasis added). Aranda teaches dividing a frame buffer into two separate devices in order to avoid using a dual port configuration, and does *not* teach a *single dual port RAM device operative to obtain pixel data from the frame buffer*. Thus, Aranda actually *teaches away from* utilizing this approach, and combining Aranda with Potter could not enable a system that utilizes a dual port RAM device, as found in the present invention.

In view of the above comments, it is readily apparent that neither Potter *et al.* nor Aranda, alone or in combination, teach or suggest the presently claimed invention as recited in independent claims 1, 21, 26, and 30 and claims 2-20, 22-25, 27-29, and 31-33, which depend respectively there from. This rejection should be withdrawn.

IX. Conclusion

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejection of claims 1-33 be reversed.

Respectfully submitted,
AMIN & TUROCY, LLP



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X. Appendix of Claims (37 C.F.R. § 1.192(c)(9))

1. (Original) A raster engine for interfacing a frame buffer in a computer system to one of a plurality of disparate displays, comprising:

at least one control register programmable via the computer system to select a display mode;

a dual port RAM device operative to obtain pixel data from the frame buffer; and

a logic device having a parallel output, the logic device being adapted to select appropriate pixel data from the dual port RAM device according to the selected display mode, to remap the selected pixel data according to the selected display mode, and to provide remapped selected pixel data at the parallel output according to a universal routing scheme applicable to the plurality of disparate displays.

2. (Original) The raster engine of claim 1, wherein the selected display mode comprises one of single pixel per clock up to 24 bits wide, single 16 bit 565 pixel per clock, single 16 bit 555 pixel per clock, single 24 bit pixel on 18 lines, single 16 bit 565 pixel on 18 lines, single 16 bit 555 pixel on 18 lines, 2 pixels per clock, 4 pixels per clock, 8 pixels per shift clock, 2 2/3 pixels per clock, and dual 2 2/3 pixels per clock.

3. (Original) The raster engine of claim 2, further comprising one of a look up table, a grayscale generator, and a blink logic system, wherein the logic device receives the selected pixel data from the dual port RAM device via the one of the look up table, the grayscale generator, and the blink logic system according to the selected display mode.

4. (Original) The raster engine of claim 3, wherein the logic device comprises a multiplexer.

5. (Original) The raster engine of claim 1, wherein the logic device is adapted to provide the selected pixel data to the output device in a 24 bit parallel format when the selected

display mode is one of single 16 bit 565 pixel per clock and single 16 bit 555 pixel per clock.

6. (Original) The raster engine of claim 5, wherein the logic device is further adapted to copy a plurality of most significant bits from the selected pixel data into a corresponding plurality of unused least significant bits in the 24 bit parallel format, whereby improved color intensity range is provided.

7. (Original) The raster engine of claim 6, further comprising one of a look up table, a grayscale generator, and a blink logic system, wherein the logic device receives the selected pixel data from the dual port RAM device via the one of the look up table, the grayscale generator, and the blink logic system.

8. (Original) The raster engine of claim 7, wherein the logic device comprises a multiplexer.

9. (Original) The raster engine of claim 1, further comprising one of a look up table, a grayscale generator, and a blink logic system, wherein the logic device receives the selected pixel data from the dual port RAM device via the one of the look up table, the grayscale generator, and the blink logic system.

10. (Original) The raster engine of claim 1, wherein the selected display mode comprises a color mode, a shift mode, and a pixel mode.

11. (Original) The raster engine of claim 10, wherein the color mode comprises one of a look up table mode, triple 8 bits per channel, 16 bit 565 color mode, 16 bit 555 color mode, and a grayscale palette enabled mode.

12. (Original) The raster engine of claim 11, wherein the shift mode comprises one of single pixel per pixel clock up to 24 bits wide, single 24 bit or 16 bit pixel mapped to 18 bits per

pixel clock, 2 pixels per shift clock up to 9 bits wide, 4 pixels per shift clock up to 4 bits wide, 8 pixels per shift clock up to 2 bits wide, 2 2/3 pixels per clock over 8 bit bus 3 bits wide, and dual 2 2/3 pixels per clock over dual 8 bit busses 3 bits wide.

13. (Original) The raster engine of claim 12, wherein the pixel mode comprises one of 4 bits per pixel, 8 bits per pixel, 16 bits per pixel, 24 bits per pixel, and 32 bits per pixel.

14. (Original) The raster engine of claim 11, wherein the pixel mode comprises one of 4 bits per pixel, 8 bits per pixel, 16 bits per pixel, 24 bits per pixel, and 32 bits per pixel.

15. (Original) The raster engine of claim 10, wherein the pixel mode comprises one of 4 bits per pixel, 8 bits per pixel, 16 bits per pixel, 24 bits per pixel, and 32 bits per pixel.

16. (Original) The raster engine of claim 15, wherein the shift mode comprises one of single pixel per pixel clock up to 24 bits wide, single 24 bit or 16 bit pixel mapped to 18 bits per pixel clock, 2 pixels per shift clock up to 9 bits wide, 4 pixels per shift clock up to 4 bits wide, 8 pixels per shift clock up to 2 bits wide, 2 2/3 pixels per clock over 8 bit bus 3 bits wide, and dual 2 2/3 pixels per clock over dual 8 bit busses 3 bits wide.

17. (Original) The raster engine of claim 10, wherein the shift mode comprises one of single pixel per pixel clock up to 24 bits wide, single 24 bit or 16 bit pixel mapped to 18 bits per pixel clock, 2 pixels per shift clock up to 9 bits wide, 4 pixels per shift clock up to 4 bits wide, 8 pixels per shift clock up to 2 bits wide, 2 2/3 pixels per clock over 8 bit bus 3 bits wide, and dual 2 2/3 pixels per clock over dual 8 bit busses 3 bits wide.

18. (Original) The raster engine of claim 13, wherein the logic device comprises a multiplexer.

19. (Original) The raster engine of claim 1, wherein the logic device comprises a multiplexer.

20. (Original) The raster engine of claim 1, wherein the selected display mode comprises a direct display command interface.

21. (Original) A raster engine for interfacing a frame buffer in a computer system to one of a plurality of disparate displays, comprising:

at least one control register programmable via the computer system to indicate a selected display mode;

means for programming the at least one control register;

means for selecting appropriate pixel data from the frame buffer according to the selected display mode; and

means for providing the selected pixel data to an output device according to the selected display mode.

22. (Original) The raster engine of claim 21, wherein the means for selecting appropriate pixel data from the frame buffer comprises a multiplexer.

23. (Original) The raster engine of claim 21, wherein the logic device is adapted to translate the selected pixel data from a first format to a second format according to the selected display mode.

24. (Original) The raster engine of claim 23, wherein the first format comprises more bits than the second format, and wherein the logic device is adapted to interpolate between a portion of the selected pixel data in the first format to generate a portion of the data in the second format.

25. (Original) The raster engine of claim 24, wherein the logic device is adapted to perform a logical OR combination of at least two bits of the selected pixel data in the first format to generate a bit in the second format.

26. (Original) In a raster engine, a method of interfacing a frame buffer in a computer system to one of a plurality of disparate displays, comprising:

programming at least one control register via the computer system to indicate a selected display mode;

selecting appropriate pixel data from the frame buffer according to the selected display mode; and

providing the selected pixel data to an output device according to the selected display mode.

27. (Original) The method of claim 26, further comprising translating the selected pixel data from a first format to a second format according to the selected display mode.

28. (Original) The method of claim 27, wherein the first format comprises more bits than the second format, and wherein translating the selected pixel data from a first format to a second format comprises interpolating between a portion of the selected pixel data in the first format to generate a portion of the data in the second format.

29. (Original) The method of claim 28, further comprising performing a logical OR combination of at least two bits of the selected pixel data in the first format to generate a bit in the second format.

30. (Original) A raster engine for interfacing a frame buffer in a computer system to a display, comprising:

at least one control register programmable via the computer system to indicate a selected display mode;

means for selecting appropriate pixel data from the frame buffer and providing the selected pixel data to an output device according to the selected display mode.

31. (Original) The raster engine of claim 30, further comprising means for translating the selected pixel data from a first format to a second format according to the selected display

mode.

32. (Original) The raster engine of claim 31, wherein the first format comprises more bits than the second format, further comprising means for interpolating between a portion of the selected pixel data in the first format to generate a portion of the data in the second format.

33. (Original) The raster engine of claim 32, further comprising means for performing a logical OR combination of at least two bits of the selected pixel data in the first format to generate a bit in the second format.